

JEDEC STANDARD

DDR4 SDRAM

JESD79-4B

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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DDR4 SDRAM STANDARD

(From JEDEC Board Ballot JCB-16-56, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

Each aspect of the changes for DDR4 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JEDEC Standard, JESD79-4, replacing whole sections and incorporating the changes into Functional Description and Operation.

2 DDR4 SDRAM Package Pinout and Addressing

2.1 DDR4 SDRAM Row for X4, X8 and X16

The DDR4 SDRAM x4/x8 component will have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

The DDR4 SDRAM x16 component will have 16 electrical rows of balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR4 SDRAM Ball Pitch

The DDR4 SDRAM component will use a ball pitch of 0.8 mm by 0.8 mm. The number of depopulated columns is 3.

2.3 DDR4 SDRAM Columns for X4,X8 and X16

The DDR4 SDRAM x4/x8 and x16 component will have 6 electrical columns of balls in 2 sets of 3 columns. There will be columns between the electrical columns where there are no balls populated. The number of these columns is 3.

Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR4 SDRAM X4/8 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c ³				DM_n, DBI_n TDQS_t ² , (NC) ¹	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4 (NC) ¹	DQ2				DQ3	DQ5 (NC) ¹	VSSQ	D
E	VSS	VDDQ	DQ6 (NC) ¹				DQ7 (NC) ¹	VDDQ	VSS	E
F	VDD	(C2) ⁵ ODT1 ⁶	ODT				CK_t	CK_c	VDD	F
G	VSS	(C0) ⁵ CKE1 ⁶	CKE				CS_n	(C1) ⁵ (CS1_n) ⁶	TEN (NC) ⁷	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17 (NC) ⁴	A13	VDD	N

NOTE 1 These pins are not connected for the X4 configuration.

NOTE 2 TDQS_t is not valid for the x4 configuration.

NOTE 3 TDQS_c is not valid for the x4 configuration.

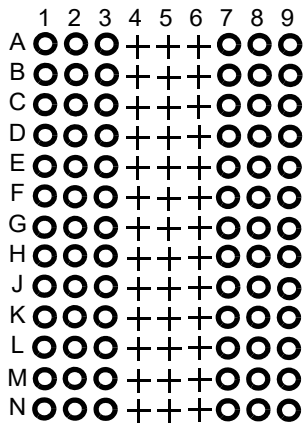
NOTE 4 A17 is only defined for the x4 configuration.

NOTE 5 These pins are for stacked component such as 3DS. For mono package, these pins are NC.

NOTE 6 ODT1 / CKE1 / CS1_n are used together only for DDP.

NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

MO-207 Variation DT-z (x4)



○ Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4)
with support balls

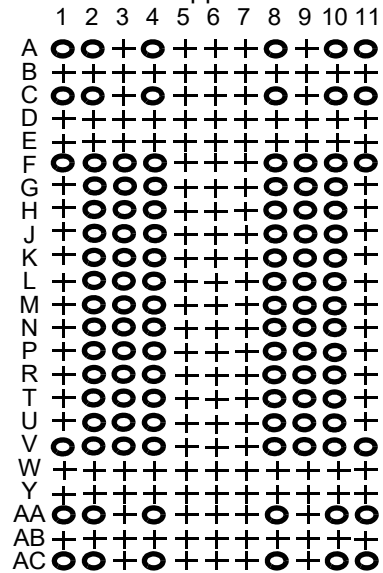


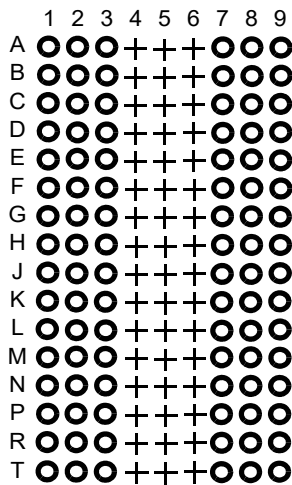
Figure
D
D

R4 Ball Assignments for the x4/8 component

2.5 DDR4 SDRAM X16 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

MO - 207 Variation DU-z (x16)



○ Populated ball
+ Ball not populated

MO-207 Variation DY-z (x16)
with support balls

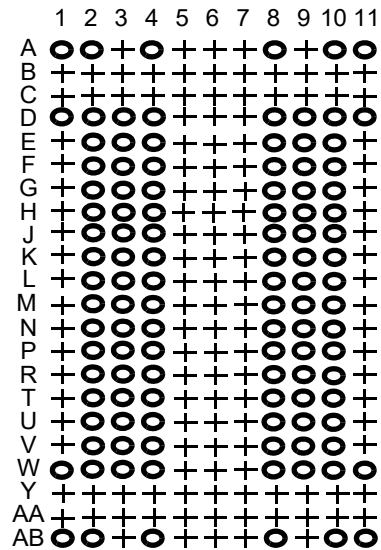


Figure 2 — DDR4 Ball Assignments for the x16 component

2.6 DDR4 SDRAM X32 Ballout using MO-XXX

The DDR4 SDRAM x32 component will have the pin assignments as defined in Figure 3. Blank cells are no ball locations.

	1	2	3	4	5	6	7	8	9	10	11	
A	VPP	VDDQ	DQS0_t	DQS0_c	VDDQ		VDDQ	DQS1_c	DQS1_t	VDDQ	VDD	1
B	VSS	VSSQ	DQ0	DM0_n, DBI0_n, NC	VSSQ		VSSQ	DQ8	DQ9	VSSQ	VSS	2
C	VDD	DQ3	DQ2	DQ1				DQ10	DQ11	DQ12	VDDQ	3
D	VDDQ	DQ4	DQ5	VSSQ				VSSQ	DQ13	DQ15	VSSQ	4
E	VSSQ	DQ6	DQ7	VDDQ				VDDQ	DQ14	DM1_n, DBI1_n, NC	ZQ	5
F	VDD	ODT1	VDDQ	ODT				CLK_t	VDDQ	CS1_n	VDD	6
G	VDD	CKE1	VSS	CKE				CLK_c	VSS	TEN	VDD	7
H	VREFCA	BA0	ACT_n	WE_n/ A14				CS_n	RAS_n/ A16	BA1	RFU	8
J	VSS	A4	VSS	BG0				CAS_n/ A15	VSS	A3	VSS	9

1. ODT1, CKE1, CS1_n and ZQ1 are for packages containing two x32 die stacked. These pins are NC for all other configurations.