JEDEC STANDARD

1.8 V HIGH-SPEED LVCMOS (HS_LVCMOS) INTERFACE

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1.8 V HIGH-SPEED LVCMOS (HS_LVCMOS) INTERFACE

(From JEDEC Board Ballot JCB-18-11, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc and ac input levels, output levels, and input overshoot and undershoot specifications for the 1.8 V High-speed LVCMOS (HS_LVCMOS) interface. The non-terminated interface has a switching range that is nominally expected to be 0 V to 1.8 V.

2 1.8 V High-speed LVCMOS (HS_LVCMOS) interface specifications

2.1 Recommended DC operating conditions

Table 1 — Recommended DC operating conditions

	Min.	Typ.	Max.	Unit	
V_{DD}	1.7	1.80	1.95	V	Power Supply
NOTE If there is a VDDQ, all I/O levels are referenced to VDDQ. If there only is VDD, then all levels are referenced to VDD.					

2.2 Leakage Current

Table 2 — Leakage Current

Parameter	Min	Max	Voltage
Input leakage current	-5	5	□A
Output leakage current	-5	5	□A

2.3 Input level

Table 3 — Input level

Parameter	Symbol	Min	Max	Unit
Input HIGH level (AC)	$V_{IH(AC)}$	0.80 • V_{DD}	V_{DD} + 0.3	V
Input LOW level (AC)	$V_{IL(AC)}$	-0.3	0.20 • V_{DD}	V
Input HIGH level (DC)	$V_{IH(DC)}$	0.7 • V_{DD}	V_{DD} + 0.3	V
Input LOW level (DC)	$V_{IL(DC)}$	-0.3	0.3 • V_{DD}	V