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**Integrated circuits – Three dimensional integrated circuits –
Part 2: Alignment of stacked dies having fine pitch interconnect**

**Circuits intégrés – Circuits intégrés tridimensionnels –
Partie 2: Alignement de puces empilées à petits pas d'interconnexion**



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**INTEGRATED CIRCUITS –
THREE DIMENSIONAL INTEGRATED CIRCUITS –**
Part 2: Alignment of stacked dies having fine pitch interconnect**FOREWORD**

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1061/FDIS	47A/1065/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63011 series, published under the general title *Integrated circuits – Three dimensional integrated circuits*, can be found on the IEC website.

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INTRODUCTION

Three-dimensional (3-D) integration of integrated circuits using through-silicon via (TSV) technology is an innovative solution to simultaneously achieve a greater performance, an improved versatility and a higher density of integrated circuits without miniaturization of feature sizes on a die. Die alignment during the die bonding is the key enabler of the fine pitch 3-D wiring between vertically stacked dies for proper physical contact. Maintenance of the alignment during the bonding process and afterward is as important as the precise overlap prior to die bonding. This standard describes a method of initial alignment and maintenance of alignment throughout the die bonding process that can be involved with mechanical shaking. The initial alignment is performed using the optical means. During the maintenance period, however, relative amount of the misalignment is converted to an electrical signal for on-the-fly alignment monitoring without the visual image.

INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 2: Alignment of stacked dies having fine pitch interconnect

1 Scope

This part of IEC 63011 provides specifications of initial alignment and alignment maintenance between multiple stacked integrated circuits during the die bonding process. These specifications define the alignment keys and operating procedures of the keys. These specifications apply only if electrical coupling method of die-to-die alignment is used in the die stacking.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63011-1, *Integrated circuits – Three dimensional Integrated Circuits – Part 1: Terminology*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 63011-1 apply.

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3.1

die bonding

assembly step to adhere physically or chemically a die to another

3.2

bonder

apparatus performing die bonding

3.3

signal generator

apparatus generating electrical signals

3.4

alignment key

apparatus to monitor or adjust the alignment of the overlaid dies

3.5

aligner

apparatus to perform the alignment of the overlaid dies