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INTERNATIONAL STANDARD

NORME INTERNATIONALE

colour inside

Integrated circuits – Three dimensional integrated circuits – Part 1: Terminology

Circuits intégrés – Circuits intégrés tridimensionnels – Partie 1: Terminologie

IEC 63011-1:2018-11(en-fr)

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 1: Terminology

FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1060/FDIS	47A/1064/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63011 series, published under the general title *Integrated Circuits – Three dimensional integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

High performance electrical system requires a massive data exchange between processing integrated circuit (IC) and storage IC. Stacked multiple ICs with a large number of vertical interconnects among dies are an innovative way of providing higher data transfer rate among dies. In addition to bumps, metal pillars, or metal pads which are traditional ways of interconnection between dies, through-silicon vias enable to configure the integration of three or more dies. The integration environment of multichip IC is significantly different from that of the integration on a printed circuit board. This document describes definitions pertaining to the multichip ICs.

INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 1: Terminology

1 Scope

This part of IEC 63011 provides definitions pertaining to multichip integrated circuits, as vertically stacked dies using through-silicon vias (TSVs) or micro bumps. Terms and definitions related to the fabrication and test of the multichip integrated circuits are also provided.

2 Normative reference

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

There are no normative references in this document.

3 Terms and definitions

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- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1 General

The general terms listed below relate to the secondary integration method in vertical direction using integrated circuits fabricated on a horizontal surface of semiconductor.

3.1.1
interposer
electrical interface that connects one socket or connection to another

Note 1 to entry: The purpose of an interposer is to spread a connection to a wider pitch or to reroute a connection to a different connection

3.1.2
multichip interconnect technology
technology that allows for the vertical stacking of layers of basic electronic components which are connected using an interconnect fabric are as follows:

Note 1 to entry: "Basic electronic components" are elementary circuit devices such as transistors, diodes, resistors, capacitors and inductors.

Note 2 to entry: A special case of multichip interconnect technology is the interposer structures that may only contain interconnect layers, although in many cases other basic electronic components (in particular decoupling capacitors) may be embedded into the interposer.