

# **JEDEC PUBLICATION**

---

## **System Level ESD Part II: Implementation of Effective ESD Robust Designs**

---

**JEP162A**

(Revision of JEP162, January 2013)

**SEPTEMBER 2019**

---

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



## NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to [www.jedec.org](http://www.jedec.org) under Standards and Documents for alternative contact information.

Published by  
©JEDEC Solid State Technology Association 2019  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

**PRICE: Contact JEDEC**

Printed in the U.S.A.  
All rights reserved

PLEASE!

DON'T VIOLATE  
THE  
LAW!

This document is copyrighted by JEDEC and may not be reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association  
3103 North 10th Street  
Suite 240 South  
Arlington, VA 22201-2107

or refer to [www.jedec.org](http://www.jedec.org) under Standards-Documents/Copyright Information.

## System Level ESD

### Part II: Implementation of Effective ESD Robust Designs

#### Contents

		<b>Page</b>
Introduction .....		iii
I.1 Overview .....		iii
I.2 Understanding Component to System ESD .....		iv
I.3 Communication and Strategy .....		v
I.4 Implementation of Advanced Tools .....		v
I.5 Impact from the Technology Roadmap .....		vi
I.6 Conclusions .....		vi
1 Scope.....		1
2 References.....		1
3 Terms and Definitions.....		6
4 Background and Outline .....		11
4.1 History of the Industry Council on ESD Target Levels .....		11
4.1 History of the Industry Council on ESD Target Levels (cont'd).....		12
4.2 JEP162 (White Paper 3 Part II): Summary of Clauses/Annexes .....		12
4.2 JEP162 (White Paper 3 Part II): Summary of Clauses/Annexes (cont'd) .....		13
4.2 JEP162 (White Paper 3 Part II): Summary of Clauses/Annexes (cont'd) .....		14
5 Overview of ESD Stressing and System Response .....		15
5.1 Presently Used Stress Tests for ESD.....		15
5.1 Presently Used Stress Tests for ESD (cont'd).....		16
5.2 Definitions.....		16
5.2 Definitions (cont'd).....		17
5.3 Coupling of ESD into Systems and Circuits .....		17
5.4 Troubleshooting to Determine the Cause of Failures .....		21
5.5 New Technologies for Determining Root Cause of Failures.....		21
5.6 Summary .....		24
6 State-of-the-Art ESD/EMI Co-design.....		24
Introduction .....		24
6.1 The Basics .....		25
6.2 Advanced System ESD Protection Methods .....		33
6.3 Comprehensive Co-Design Methodologies.....		38
6.4 Conclusion .....		39
7 Reference Methodologies for IC/System Protection Co-Design.....		40
Introduction .....		40
7.1 Approaches – Categories.....		42
7.2 Examples .....		52
8 Standard Model and Analytical Tool Needs To Support SEED .....		58
Introduction .....		58
8.1 Component Characterization and Model Requirements to Support SEED Category 1 .....		59
8.2 Component Characterization and Model Requirements to Support SEED Category 2.....		68
8.3 System Characterization and Model Requirements to Support SEED Category 3 .....		69
8.4 Conclusion .....		78
9 Summary and Conclusions.....		79
Introduction .....		79
9.1 Overview of ESD Stressing and System Response - Clause 5 .....		79
9.2 State-of-the-Art ESD/EMI Co-Design - Clause 6 .....		79
9.3 Reference Methodologies for IC/System - Clause 7 .....		81
9.4 Standard Model and Analytical Tool Needs to Support SEED - Clause 8.....		82
9.5 Application Specific Information on System ESD Related Tests and Their Targets – Annex A.....		82
9.6 Technology Roadmap and Direction – Annex B .....		83

9.7 Outlook.....	84
Annex A: Application Specific Information on System ESD related Tests and their Targets .....	85
Introduction .....	85
A.1 System Tests and Targets of Mobile Phones .....	85
A.2 System Tests and Targets of Automotive Electronic Components .....	87
A.3 System Tests and Targets of Computing Devices.....	89
A.4 System Tests and Targets of Medical Electronic Components .....	90
A.5 System Tests and Targets of Avionic Components.....	91
A.6 System Tests and Targets of Consumer Electronic Devices .....	92
A.7 Applicability of System-Efficient ESD Design (SEED).....	93
Annex B: Technology Roadmap and Direction.....	95
Introduction .....	95
B.1 Roadmap for ICs: Microprocessors .....	96
B.2 Roadmap for Automotive Applications .....	98
B.3 Roadmap for IC Package and Applications .....	99
B.4 Advances in Board and Assembly Technologies .....	101
B.5 Optical Interconnects .....	104
B.6 Polymer Applications.....	104
B.7 Future Compatibility to IEC Protection Requirements .....	106
Annex C: Fast and Slow ESD Stress (High and Low Frequency Spectrum).....	109
Discussion.....	109
C.1 Some Words on ESD Debugging.....	112
Annex D: Review of JEP161 (White Paper 3 Part I).....	113
D.1 JEP161 Clause 4: Purpose and Introduction .....	113
D.2 JEP161 Clause 5: Test Methods and Their Field of Application .....	113
D.3 JEP161 Clause 6: Proven System Level Fails.....	115
D.4 JEP161 Clause 7: OEM System Level ESD Needs and Expectations .....	116
D.5 JEP161 Clause 8: Lack of Correlation between HBM/CDM and IEC 61000-4-2 .....	117
D.6 JEP161 Clause 9: Relationship between IC Protection Design and System Robustness .....	118
D.7 JEP161 Clause 10: Summary, Conclusions and Outlook.....	120
Annex E: Frequently Asked Questions.....	121
Annex F: Differences between revisions .....	127

---

## Foreword

---

This document is the second of two Electrostatic Discharge (ESD) Industry Council white papers dealing with System Level ESD (Part I is JEP161).

In JEP161, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In JEP162 we expand this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types, and describe new detection techniques, models, and improvements in design for system robustness. JEP162 also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

JEP162A begins with an overview of system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures, and provides a “cost vs. performance vs. robustness” analysis of present-day state-of-the-art electromagnetic compatibility (EMC)/electromagnetic interference (EMI) design prevention methods that have been developed to prevent system level ESD failure. It follows with an expansion of SEED failure classifications to cover a combination of hard (permanent) and/or soft (resettable) system failures and stresses which could cause these errors, and describes cases where the SEED co-design approach can be expanded to provide additional benefits to system ESD design. System design simulation tools are described in the context of their potential improvements to simulating system level ESD stress and failure modes. Application-specific industry system ESD test methods are then described in the context of their ability to reveal hard and soft failure modes from actual system deployment. Finally, a technology roadmap of the system design components is described, including IC technology and related circuit speeds, automotive electronics, packaging technology, system / board interconnect technology and ESD protection materials, illustrating continuing challenges for system ESD design improvement.

---

## Introduction

---

### I.1 Overview

JEP162A, while establishing the complex nature of System Level ESD, proposes that an **efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level**. This objective requires an appropriate characterization of the components and a methodology to assess the entire system using simulation data. This is applicable to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)). This type of systematic approach is long overdue and represents an advanced design approach which replaces the misconception, as discussed in detail in JEP161, that a system will be sufficiently robust if all components exceed a certain ESD level.

In the first step, a method for categorizing the failure types has been introduced. An advanced characterization and simulation approach is discussed through examples. However, a full design flow cannot be established without **a common effort across the electronic industry involving IC suppliers, suppliers of discrete protection components and original equipment manufacturers (OEMs) as well as tool vendors**. This paper identifies existing tools with both simulations and scanning techniques that are applicable for this purpose and calls out fields for further development.