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System Level ESD
Part II: Implementation of Effective ESD Robust Designs

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Contents

Foreword

This document is the second of two Electrostatic Discharge (ESD) Industry Council white papers dealing with System Level ESD (Part I is JEP161).

In JEP161, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In JEP162 we expand this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types, and describe new detection techniques, models, and improvements in design for system robustness. JEP162 also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

JEP162A begins with an overview of system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures, and provides a "cost vs. performance vs. robustness" analysis of present-day state-of-the-art electromagnetic compatibility (EMC)/electromagnetic interference (EMI) design prevention methods that have been developed to prevent system level ESD failure. It follows with an expansion of SEED failure classifications to cover a combination of hard (permanent) and/or soft (resettable) system failures and stresses which could cause these errors, and describes cases where the SEED co-design approach can be expanded to provide additional benefits to system ESD design. System design simulation tools are described in the context of their potential improvements to simulating system level ESD stress and failure modes. Application-specific industry system ESD test methods are then described in the context of their ability to reveal hard and soft failure modes from actual system deployment. Finally, a technology roadmap of the system design components is described, including IC technology and related circuit speeds, automotive electronics, packaging technology, system / board interconnect technology and ESD protection materials, illustrating continuing challenges for system ESD design improvement.

Introduction

I.1 Overview

JEP162A, while establishing the complex nature of System Level ESD, proposes that an **efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level**. This objective requires an appropriate characterization of the components and a methodology to assess the entire system using simulation data. This is applicable to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)). This type of systematic approach is long overdue and represents an advanced design approach which replaces the misconception, as discussed in detail in JEP161, that a system will be sufficiently robust if all components exceed a certain ESD level.

In the first step, a method for categorizing the failure types has been introduced. An advanced characterization and simulation approach is discussed through examples. However, a full design flow cannot be established without **a common effort across the electronic industry involving IC suppliers, suppliers of discrete protection components and original equipment manufacturers (OEMs) as well as tool vendors**. This paper identifies existing tools with both simulations and scanning techniques that are applicable for this purpose and calls out fields for further development.