INCH-POUND

The documentation and process conversion measures necessary to comply with this document shall be completed by 4 September 2019.

MIL-PRF-19500/534J
4 June 2019
SUPERSEDING
MIL-PRF-19500/534H
14 November 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, POWER, TYPES 2N5002 AND 2N5004, ENCAPSULATED (CASE MOUNT PACKAGE) AND UNENCAPSULATED, RADIATION HARDNESS ASSURANCE, QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors for use in high-speed power-switching applications. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device type as specified in MIL-PRF-19500. Two levels of product assurance (JANHC and JANKC) for each unencapsulated device type die.

1.2 Physical dimensions.

1.2.1 Package outlines. The device package outline is a TO-210AA (formerly TO-59) in accordance with figure 1 for all encapsulated device types.

1.2.2 Unencapsulated die. The dimensions and topography for JANHC and JANKC unencapsulated die are in accordance with figure 2.

1.3 Maximum ratings. Unless otherwise specified T_A = +25°C.

P_T (1) T_A = 25°C	P_T (2) T_C = 25°C	$R_{\theta JA}$	$R_{\theta JC}$ (3)	V_{CBO}	V_{CEO}	V_{EBO}	I_C	I_C (4)	Reverse pulse energy (5)	T_{stg} and T_J
W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	mJ	°C
2	58	88	3	100	80	5.5	5	10	15	−65 to +200

(1) Derate linearly 11.4 mW/°C for T_A > 25°C.
(2) For derating see figure 3.
(3) For thermal impedance see figure 4.
(4) This value applies for Pw ≤ 8.3 ms, duty cycle ≤ 1 percent.
(5) This rating is based on the capability of the transistors to operate safely in the unclamped inductive load energy test circuit figure 5 herein.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

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