

INTERNATIONAL STANDARD

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Test methods for electrical materials, printed boards and other interconnection structures and assemblies –

Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles –

Partie 5-501: Méthodes d'essai générales pour les matériaux et les ensembles – Essais de résistance d'isolement en surface (RIS) des flux de brasage



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS
AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –****Part 5-501: General test methods for materials and assemblies –
Surface insulation resistance (SIR) testing of solder fluxes**

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IEC 61189-5-501 has been prepared by IEC technical committee 91: Electronics assembly technology. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
91/1645/CDV	91/1672/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies*, can be found on the IEC website.

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 5-501: General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes

1 Scope

This part of IEC 61189 is used to quantify the deleterious effects of flux residues on surface insulation resistance (SIR) in the presence of moisture.

Interdigitated comb patterns comprising long parallel electrodes on an IPC B53 standardized test coupon are used for the evaluation. Coupons are conditioned and measurements taken at a high temperature and humidity. The electrodes are electrically biased during conditioning to facilitate electrochemical reactions, as shown in Figure 1 and Figure 3.

Reference can be made to IEC TR 61189-5-506, which examines different geometry comb patterns: 400 μm x 500 μm ; 400 μm x 200 μm ; and 318 μm x 318 μm .

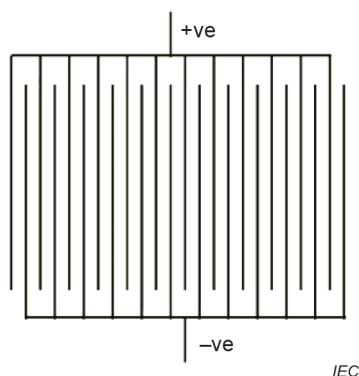


Figure 1 – SIR pattern

Specifically, this method is designed to simultaneously assess:

- leakage current caused by ionized water films and electrochemical degradation of test vehicle, (corrosion, dendritic growth);
- provide metrics that can appropriately be used for binary classification (e.g. go/no go; pass/fail);
- compare, rank or characterize materials and processes.

This test is carried out at high humidity and heat conditions.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-1:2013, *Environmental testing – Part 1: General and guidance*

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60068-2-67, *Environmental testing – Part 2-67: Tests – Test Cy: Damp heat, steady state, accelerated test primarily intended for components*