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SystemVerilog – Unified Hardware Design, Specification, and Verification Language

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Contents

Part One: Design and Verification Constructs

Part Two: Hierarchy Constructs

Part Three: Application Programming Interfaces

List of figures

List of tables

List of syntax excerpts

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IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society
and the
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IEEE-SA Standards Board

Abstract: The definition of the language syntax and semantics for SystemVerilog, which is a unified hardware design, specification, and verification language, is provided. This standard includes support for modeling hardware at the behavioral, register transfer level (RTL), and gate-level abstraction levels, and for writing testbenches using coverage, assertions, object-oriented programming, and constrained random verification. The standard also provides application programming interfaces (APIs) to foreign programming languages.

Keywords: assertions, design automation, design verification, hardware description language, HDL, HDVL, IEEE 1800™, PLI, programming language interface, SystemVerilog, Verilog®, VPI