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# **INTERNATIONAL IEEE Std 1800.2™ STANDARD**

**SystemVerilog –  
Part 2: Universal Verification Methodology Language Reference Manual**





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IEC Central Office  
3, rue de Varembe  
CH-1211 Geneva 20  
Switzerland  
Tel.: +41 22 919 02 11  
[info@iec.ch](mailto:info@iec.ch)  
[www.iec.ch](http://www.iec.ch)

Institute of Electrical and Electronics Engineers, Inc.  
3 Park Avenue  
New York, NY 10016-5997  
United States of America  
[stds.info@ieee.org](mailto:stds.info@ieee.org)  
[www.ieee.org](http://www.ieee.org)

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Part 2: Universal Verification Methodology Language Reference Manual**

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## SystemVerilog –

### Part 2: Universal Verification Methodology Language Reference Manual

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Full information on the voting for its approval can be found in the report on voting indicated in the above table.

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# IEEE Standard for Universal Verification Methodology Language Reference Manual

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Grateful acknowledgment is made for permission to use the following source material:

Accellera Systems Initiative—*The Universal Verification Methodology (UVM)*  
*pre-IEEE Class Reference.*

**Abstract:** The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.

**Keywords:** agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction level modeling, verification methodology