IEC 62530-2

Edition 1.0 2021-07

INTERNATIONAL STANDARD IEEE Std 1800.2™

SystemVerilog –
Part 2: Universal Verification Methodology Language Reference Manual

IEC 62530-2:2021-07(en) IEEE Std 1800.2-2017

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 25.040.01; 35.060

ISBN 978-2-8322-9974-6

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The text of this International Standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1800.2 (2017)	91/1713/FDIS	91/1725/RVD

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IEEE Std 1800.2™-2017

IEEE Standard for Universal Verification Methodology Language Reference Manual

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Design Automation Standards Committee
of the
IEEE Computer Society

Approved 14 February 2017

IEEE-SA Standards Board

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Accellera Systems Initiative—*The Universal Verification Methodology (UVM) pre-IEEE Class Reference*.

Abstract: The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.

Keywords: agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction level modeling, verification methodology